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# Comparison of CMOS and Adiabatic Full Adder Circuits

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**Abstract**— Full adders are important components in applications such as digital signal processors (DSP) architectures and microprocessors. Apart from the basic addition adders also used in performing useful operations such as subtraction, multiplication, division, address calculation, etc. In most of these systems the adder lies in the critical path that determines the overall performance of the system. In this paper conventional complementary metal oxide semiconductor (CMOS) and adiabatic adder circuits are analyzed in terms of power and transistor count in 0.18um technology.

**Index Terms**— Low-power, adiabatic logic, Full adder, CMOS, Pass transistor logic, Positive feed back adiabatic logic, Transmission gate logic

## 1 INTRODUCTION

Power minimization is one of the primary concerns in today VLSI design methodologies because of two main reasons one is the long battery operating life requirement of mobile and portable devices and second is due to increasing number of transistors on a single chip leads to high power dissipation and it can lead to reliability and IC packaging problems.

Power dissipation can be reduced by employing different techniques at different levels of abstraction of the IC design process (system, algorithmic, architecture et al.). At the circuit level, power dissipation in CMOS Logic is related to $kCV^2$ where k is switching activity, C is load capacitance and V represents supply voltage. General approaches for reducing power consumption at circuit level are reducing the power supply voltage, reducing switching activity or reducing load capacitance [1],[2]. Another approach for reducing power dissipation at the circuit level is usage of AC power supply for recycling energy of node capacitances. The principle is known as adiabatic which is taken from thermodynamics. In literature, there are two kinds of adiabatic circuits presented one is full-adiabatic and other is quasi-adiabatic or partial adiabatic circuits. [1]

Addition is one of the important and commonly used arithmetic operation in many signal processing and other applications. So, an adder is one of the most critical components of a processor which determines its throughput, as it is used in the ALU, the floating-point unit, and for address generation in case of cache or memory access. In this paper we present different full adder designs based on adiabatic and conventional CMOS logic principle and their performance based on the power dissipation compared.

The rest of the paper is organized as follows. Section 2 gives details of conventional charging and adiabatic charging principle, Section 3 explains different full adder implementations, section 4 simulation results and finally sec 5 is conclusion.

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## 2. ADIABATIC PRINCIPLE

The operation of adiabatic logic gate is divided into two distinct stages: one stage is used for logic evaluation; the other stage is used to reset the gate output logic value. Both the stages utilize adiabatic switching principle. In the following section conventional switching and adiabatic switching analyzed in detail.

### 2.1 Conventional Charging

There are three major sources of power dissipation in digital CMOS circuits those are dynamic, short circuit and leakage power dissipation. The dominant component is dynamic power dissipation and is due to charging, discharging of load capacitance [2]. The equivalent circuits of CMOS logic for charging and discharging is shown in Fig.1. The expression for total power dissipation is given by.

$$P_{tot} = \alpha.C_L.V.V_{DD}.f_{clk} + I_{SC}.V_{DD} + I_{le}.V_{DD} \quad (1)$$

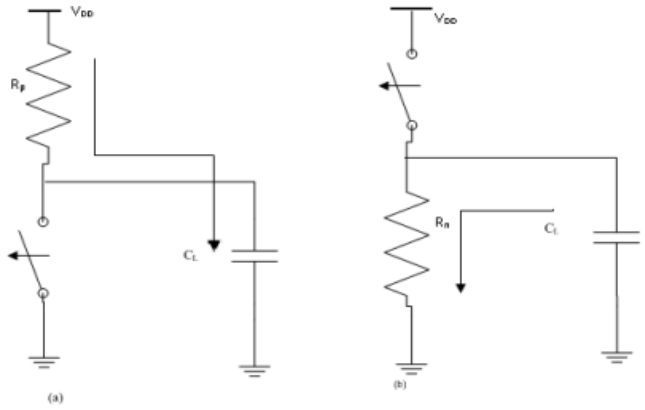


Fig.1. Conventional CMOS a) Charging b) Discharging

Equation (1), the first term represents the dynamic power, where CL is the loading capacitance, fclk is the clock frequency, and α is the switching activity. In most cases, the voltage swing V is the same as the supply voltage Vdd; however, in some logic circuits, the voltage swing on some internal nodes may be slightly less. The second term is due to the direct-path short circuit current Isc which arises when both the NMOS and PMOS transistors are simultaneously active, conducting current directly from supply to ground. Finally, leakage current Ile which can arise from substrate injection and sub threshold effects is primarily determined by fabrication technology considerations. [2], [4]

### 2.2 Adiabatic Switching

Adiabatic switching can be achieved by ensuring that the potential across the switching devices is kept arbitrarily small. This can be achieved by charging the capacitor from a time-varying voltage source or constant current source [1], [4], [9], as shown in Fig. 2. Here, R represents the on-resistance of the pMOS network. Also note that a constant charging current corresponds to a linear voltage ramp.

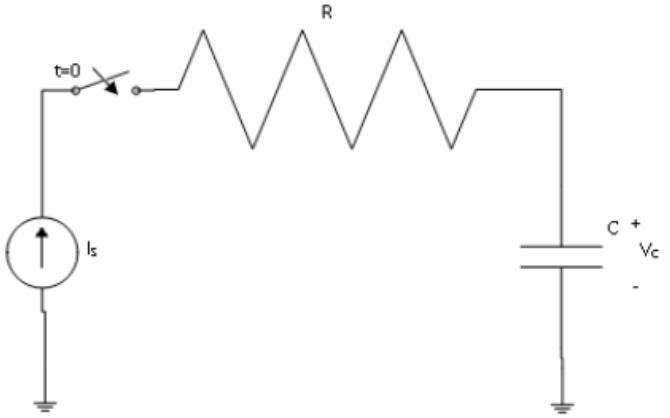


Fig .2.adiabatic charging principle

Assuming that the capacitance voltage $V_C$ is zero initially, the variation of the voltage as a function of time can be found as

$$V_C(t) = I_S.t/C \quad (2)$$

Hence the charging current can be expressed as a function of $V_C$ and time t

$$I_S = C.V_C(t)/t \quad (3)$$

The amount of energy dissipated in the resistor R from t = 0 to *t* = T can be found as

$$E_{diss} = R\int_0^T I_S^2 dt = RI_S^2 T \quad (4)$$

Combining (3) and (4), the dissipated energy during this charge-up transition can also be expressed as

$$E_{diss} = \frac{RC}{T}.CV_C^2(T) \quad (5)$$

From (5) we can say that the dissipated energy is smaller than for the conventional case if the charging time T >>2RC and can be made small by increasing the charging time. A portion of the energy thus stored in the capacitance can also be reclaimed by reversing the current source direction, allowing the charge to be transferred from the capacitance back into the supply. Adiabatic logic circuits thus require non-standard power supplies with time-varying voltage, also called pulsed power supplies. The additional hardware overhead associated with these specific power supply circuits is one of the design trade-off. Practical supplies can be constructed by using resonant inductor circuits. But the use of inductors should be limited from integrated circuit point because of so many factors like chip integration, accuracy, efficiency etc. [4]

An alternative to using pure voltage ramps is to use stepwise supply voltage waveforms, where the output voltage of the power supply is increased and decreased in small increments during charging and discharging. Since the energy dissipation depends on the average voltage drop across the resistor by using smaller voltage steps the dissipation can be reduced considerably [4]. The total dissipation using step wise charging is given by (6)

$$E_{tdiss} = \frac{1}{n} C V_{DD}^2/2 \quad (6)$$

Where n is number of steps used to charge up capacitance to $V_{DD}$.

In literature, adiabatic logic circuits classified into two types: full adiabatic and quasi or partial adiabatic circuits. Full-adiabatic circuits have no non-adiabatic loss, hut they are much more complex than quasi-adiabatic circuits. Quasi-adiabatic circuits have simple architecture and power clock system. There are two types of energy loss in quasi-adiabatic circuits, adiabatic loss and nonadiabatic loss. The adiabatic loss occurs when current flows through non-ideal switch, which is proportional to the frequency of the power-clock. If any voltage difference between the two terminals of a switch exists when it is turned on, non-adiabatic loss occurs. The non-adiabatic loss, which is independent of the frequency of the power-clock, is proportional to the node capacitance and the square of the voltage difference. Several quasi-adiabatic logic architectures have been reported, such as ECRL, 2N-2N-2P, PFAL etc.

## 3 ADDER IMPLEMENTATION

A basic cell in digital computing systems is the 1-bit full adder which has three 1-bit inputs (A, B, and C) and two 1-bit outputs (*sum* and *carry*). The relations between the inputs and the outputs are expressed as

$$Sum = \bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}\bar{C} + ABC \quad (7a)$$

$$Carry = AB + BC + CA \quad (7b)$$

### 3.1 Conventional adder [2], [4], [6]

Conventional CMOS Implementation consists of two functional blocks pull-up and pull-down. Pull-up functional block is implemented with P-channel MOS transistors and pull-down functional block is implemented with N-channel MOS transistors. In order to get symmetrical structure (7a) is rearranged as (8) and sum and carry implementation is shown

in Fig.3.

$$Sum = ABC + (A + B + C)\overline{Carry} \quad (8)$$

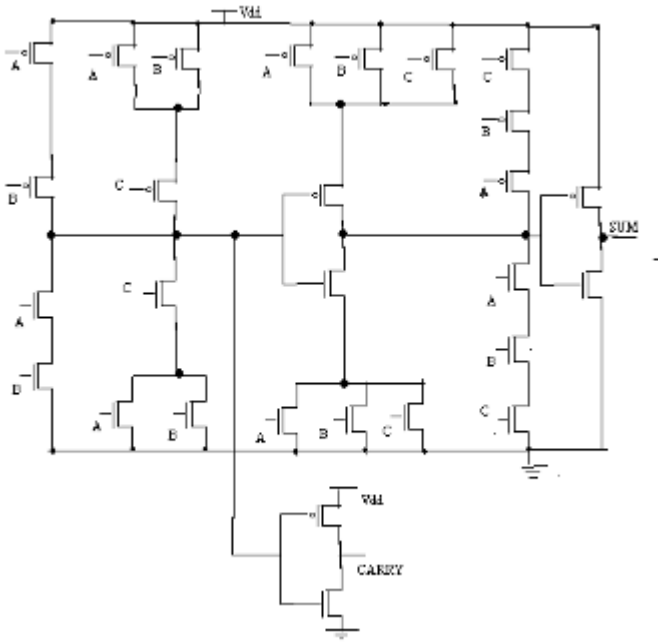


Fig.3. Conventional CMOS full adder

### 3.2 Pass transistor logic (PL) based adder [6]

Pass transistor logic is one of the well known nMOS logic style used to implement different functions. General method for deriving pass transistor logic diagram for a function is choosing control variable and pass variable based on the functional description. Adder implementation based on pass transistor principle is shown in Fig.4.

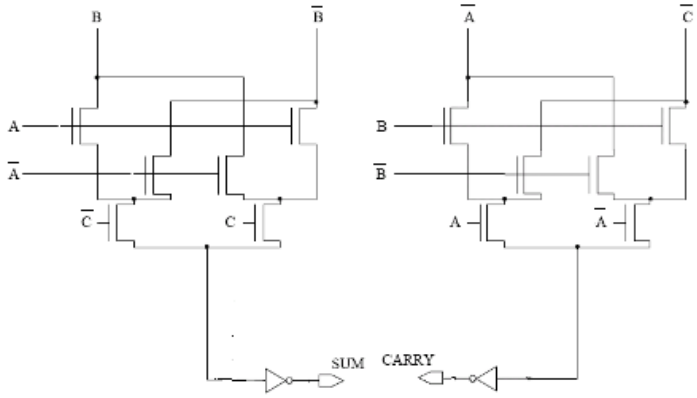


Fig.4.Pass transistor based full adder

### 3.3 Transmission gate (TG) based adder [4]

Transmission gate approach is another widely used CMOS design style to implement digital function. Transmission gate based implementation is similar to pass transistor with the difference that transmission gate logic uses nMOS and pMOS transistors where as pass transistor logic uses only one type of transistor i.e. either nMOS or pMOS. Full adder implementation based on TG logic is shown in Fig.5. [4]

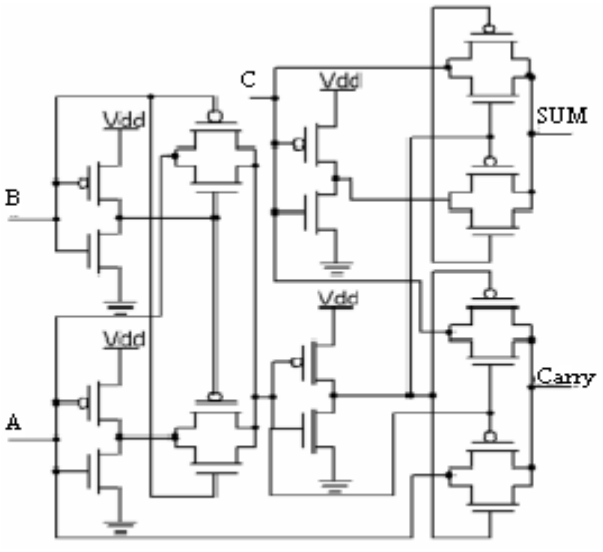


Fig.5. Transmission gate based full adder

### 3.4 Pass transistor based adiabatic adder [7]

The sum and carry expressions for one bit full adder is given by

$$Sum = A \oplus B \oplus C$$

$$Carry = AB + BC + CA \quad (9)$$

The above equations can be re arranged as

$$Sum = (A \oplus B)\overline{C} + \overline{(A \oplus B)}C$$

$$Carry = (A \oplus B)C + \overline{(A \oplus B)}B \quad (10)$$

The sum and carry expressions in (10) have common terms and can be implemented using Fig.6. [7]

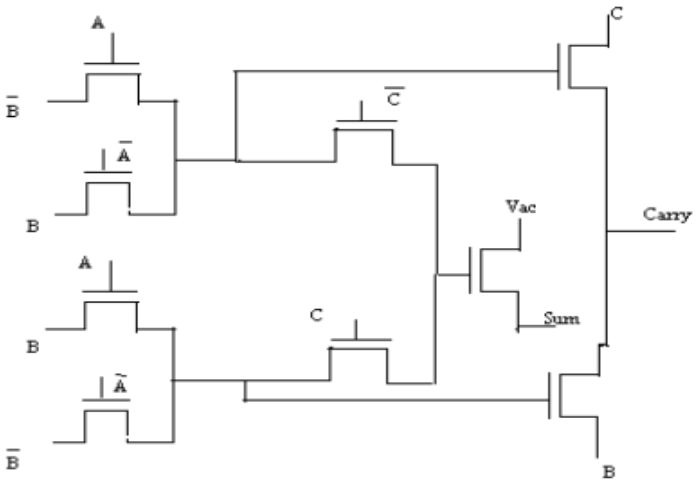


Fig.6. Pass transistor based adiabatic full adder

### 3.5 Posittive feedback adiabatic logic (PFAL) adder

The general PFAL gate consists of a two cross coupled inverters and two functional blocks F and /F (complement of F) driven by normal and complemented inputs which realizes both

normal and complemented outputs. Both the functional blocks implemented with n channel MOS transistors. The equations used to implement PFAL adder given by (11) and the corresponding sum and carry implementations are shown in Fig.7a and Fig.7b

$$Sum = \bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}\bar{C} + ABC$$

$$Carry = AB + BC + CA \qquad (11)$$

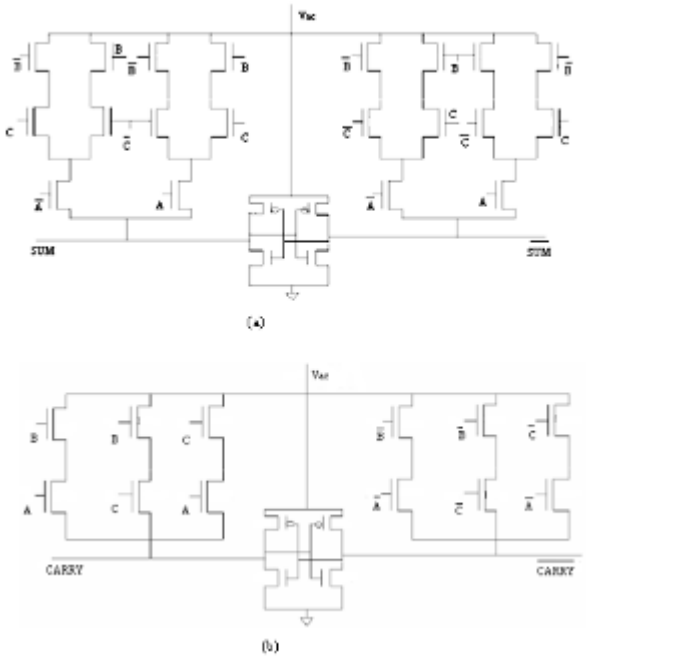


Fig.7.Positive feedback based adiabatic logic a)sum cell b)carry cell

### 3.6 Transmission gate based adiabatic adder (TGAL)

The general block diagram of transmission gate based adiabatic logic consists of two functional blocks F and complement of F operated with single clock power supply. Both normal and complemented inputs are available to functional blocks. Functional blocks are implemented using transmission gate or pass gate. The sum and carry implementation using transmission gate logic is shown in Fig .8a and Fig.8b. [4], [11]

## 4 SIMULATION RESULTS

In order to estimate the power dissipation of the different circuits present in previous section we used power meter simulation model present in [4] and RC model present in [10].All the circuits are designed in Tanner tools(S-edit,T-SPICE) using 0.18um technology parameters.Table.I gives power dissipation values under the operating conditions $V_{DD}$=1.8V,$C_L$=20fF and frequency 50MHz.Fig.9 shows the variation of power dissipation with the frequency for the different circuit implementations presented in previous section and it confirms that adiabatic logic circuits consume less power than CMOS circuits.

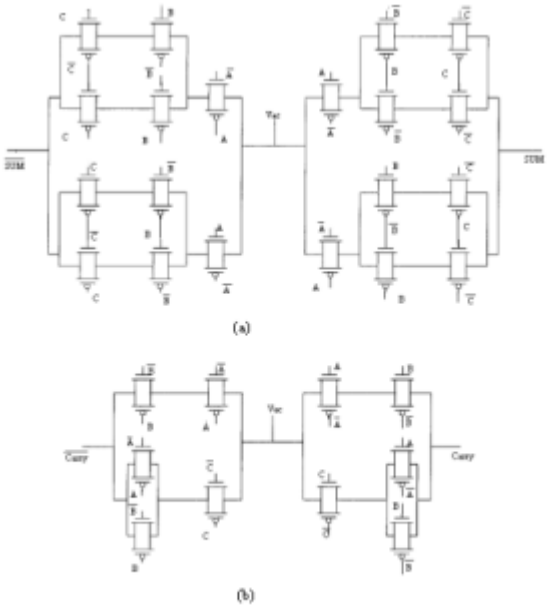


Fig.8. Trasmission gate based adiabatic logic a) sum cell b) carry cell

TABLE 1POWER DISSIPATION OF VARIOUS ADDERS UNDER THE OPERATING CONDITIONS ($V_{DD}$=1.8V,$C_L$=20FF,$F_{CLK}$=50MHz)

| Parameter | Adder type | | | | | |
|---|---|---|---|---|---|---|
| | CMOS | PL | TGL | PAL | PFAL | TGAL |
| Transistor count | 28 | 22 | 20 | 10 | 38 | 60 |
| Power dissipation(µw) | 1.9 | 1.2 | 2.1 | 0.06 | 0.05 | 0.85 |

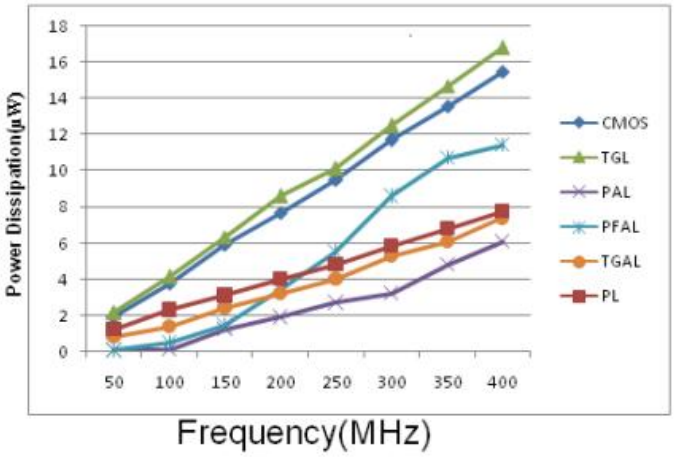


Fig.9. variation of power dissipation with frequency

## 5 CONCLUSION

In this paper we compared the performance of different adiabatic logic adder circuits with traditional CMOS adder circuits. The simulation results show that designs based on adiabatic principle gives superior performance when compared to traditional approaches in terms of power even though their transistor count is high in some circuits.

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